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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/724,189	12/01/2003	Takahiro Bokui	60188-722	1320

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EXAMINER	
WACHSMAN, HAL D	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 03/28/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/724,189	BOKUI ET AL.	
	Examiner	Art Unit	
	Hal D. Wachsman	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *21* is/are allowed.

6)☒ Claim(s) *1,2,7-9 and 15* is/are rejected.

7)☒ Claim(s) *3-6,10-14 and 16-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 January 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11-10-05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Page 2, line 4, of the specification cites "filer circuit 52" which it appears should be "filter circuit 52".

2. The replacement drawing sheets for Figures 10-12 have been approved.

3. Claims 1-21 are objected to under 37 C.F.R. 1.75(a) for failing to particularly point out and distinctly claim the subject matter which the applicant regards as the invention. Claim 1, lines 10-11, cite "the semiconductor circuit" however the antecedent basis is "semiconductor integrated circuit". Claim 1, lines 22-23, cite "the voltages of the reference parameter component" which it appears should be "the voltage of the reference parameter component". Claim 11, line 3, cites "the first and second switching circuit" which it appears should be "the first and second switching circuits". Claims 19 and 20, lines 4-5, cite "the *continuous* unit parameter components" which lacks clear antecedent basis. Claim 21, line 16, cites "the parameter value of the variable parameter" which it appears should be "the parameter value of the variable parameter component". The examiner asks the applicant to better claim the limitations cited above. While the examiner understands the intentions of the applicant he feels confusion could be drawn from the limitations cited above. Appropriate correction is required.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1, 2, 7-9 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsukawa et al. (JP 07-055588, see translation) in view of the Applicant's Admissions of the prior art.

As per claim 1, Matsukawa et al. (pages 3, 4) disclose "a current supply circuit". Matsukawa et al. (figure 2, page 4) disclose "a variable parameter component". Matsukawa et al. (see at least figures 1, 2) disclose "a plurality of switching circuits". Matsukawa et al. (figure 2, page 5) disclose "a voltage measuring circuit". Matsukawa et al. (figure 2, pages 8, 9, 17) disclose "an adjusting circuit that adjusts a parameter value of the variable parameter component". Matsukawa et al. (pages 3-5, 12, 13) disclose "any one of the switching circuits is connected to a reference parameter component having a preliminarily known parameter value". Matsukawa et al. (see at least figure 2) disclose "the switching circuits are allowed to switch electrical connections...the variable parameter component and the voltage measuring circuit". Matsukawa et al. (figure 2,

pages 11, 13, 14) disclose "the voltage measuring circuit measures voltages generated..from the current supply circuit". Matsukawa et al. (figure 2, pages 3, 4, 8-12) disclose "the adjusting circuit adjusts the parameter value of the variable parameter component...reaches the voltages of the reference parameter component". With respect to "the current supply circuit, the variable parameter component....are included in the semiconductor circuit" the various circuits/components cited here have already been addressed above. It appears though that Matsukawa et al. does not explicitly state that the circuits/components are included in a semiconductor circuit. However, the Applicants Admissions of the prior art (page 3, lines 1-5, of the specification) teach this excepted feature. Also, with respect to making these circuits/components integral with the semiconductor circuit, the Examiner respectfully notes "In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965)" in which the court affirmed the rejection holding, among other reasons, "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice". In addition, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of the Applicant's Admissions of the prior art to the invention of Matsukawa et al. as specified above because the placement of all the desired circuitry on a single semiconductor circuit would result in improved economy of size.

As per claim 2, Matsukawa et al. (figure 2, page 11) disclose the feature of this claim.

As per claim 7, Matsukawa et al. (pages 3-5, 12, 13) disclose the reference parameter component but does not explicitly disclose the including of the component in a semiconductor integrated circuit. However, the Applicants Admissions of the prior art (page 3, lines 1-5, of the specification) teach this excepted feature. Also, with respect to making these circuits/components integral with the semiconductor circuit, the Examiner respectfully notes "In re Larson, 340 F.2d 965, 968, 144 USPQ 347, 349 (CCPA 1965)" in which the court affirmed the rejection holding, among other reasons, "that the use of a one piece construction instead of the structure disclosed in [the prior art] would be merely a matter of obvious engineering choice". In addition, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of the Applicant's Admissions of the prior art to the invention of Matsukawa et al. as specified above because the placement of all the desired circuitry on a single semiconductor circuit would result in improved economy of size.

As per claim 8, the Applicant's Admissions of the prior art (figure 10, page 1, lines 12-18, page 2 lines 2-13, page 3 lines 1-5 of the specification) teach the features of this claim. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of the Applicant's Admissions of the prior art to the invention of Matsukawa et al. as specified above because both Matsukawa et al. and the Applicant's Admissions of the prior art are directed toward parameter correction techniques involving a variable resistance.

As per claim 9, the Applicant's Admissions of the prior art (figure 12, page 3, lines 20-25, page 4, lines 1-6) teach the feature of this claim. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to apply the techniques of the Applicant's Admissions of the prior art to the invention of Matsukawa et al. as specified above because both Matsukawa et al. and the Applicant's Admissions of the prior art are directed toward parameter correction techniques involving a variable resistance.

As per claim 15, Matsukawa et al. (see at least figure 2) disclose the feature of this claim.

6. Claim 21 is allowed subject to the appropriate correction of the 37 C.F.R. 1.75(a) objections noted in paragraph 3 above.

Claims 3-6, 10-14 and 16-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and subject to the appropriate correction of the 37 C.F.R. 1.75(a) objections noted in paragraph 3 above.

7. The following reference is cited as being art of general interest: Translation of JP 04-137902 (Ogata et al.) which disclose an automatic phase control circuit and detection circuit.

8. Applicant's arguments with respect to the claims rejected above have been considered but are moot in view of the new ground(s) of rejection.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hal D. Wachsman whose telephone number is 571-272-

2225. The examiner can normally be reached on Monday to Friday 7:00 A.M. to 4:30 P.M..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 571-272-2216. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hal D Wachsman
Primary Examiner
Art Unit 2857

HW
March 22, 2006